Claims

We claim:

1. A heterojunction bipolar transistor (HBT), comprising:

a collector formed over a substrate;

a base formed over the collector;

an emitter formed over the base; and

a tunneling suppression layer between the collector and the base, the tunneling suppression layer fabricated from a material that is different from a material of the base and that has an electron affinity equal to or greater than an electron affinity of the material of the base.

2. The HBT of claim 1, in which the collector comprises indium phosphide, the base comprises gallium arsenide antimonide, the emitter comprises two or more of indium, phosphorous, aluminum, gallium, nitrogen and arsenic, and the tunneling suppression layer is a material comprising two or more of aluminum, gallium, indium, nitrogen, phosphorous, arsenic and antimony.

3. The HBT of claim 2, in which the tunneling suppression layer comprises aluminum gallium indium arsenide.

4. The HBT of claim 3, in which the tunneling suppression layer comprises $Al_{0.33}Ga_{0.15}In_{0.52}As$.

5. The HBT of claim 3, in which the tunneling suppression layer consists essentially of $Al_{1-x-y}Ga_xIn_yAs$, where $0.09 \leq x \leq 0.25$, and $y=0.52$.

6. The HBT of claim 3, in which the tunneling suppression layer is structured to provide a graded electron affinity, χ.

7. The HBT of claim 6, in which the tunneling suppression layer consists essentially of $Al_{1-x-y}Ga_xIn_yAs$, where $0.09 \leq x \leq 0.25$, and $y=0.52$ and has a greater gallium mole-fraction near the collector than near the base.

8. The HBT of claim 2, in which the tunneling suppression layer comprises aluminum indium arsenide phosphide.

9. The HBT of claim 8, in which the tunneling suppression layer comprises indium phosphide and aluminum indium arsenide having between 40% and 100% indium phosphide.

10. The HBT of claim 9, in which the tunneling suppression layer comprises indium phosphide and aluminum indium arsenide having 58% indium phosphide and 42% aluminum indium arsenide near the base and 75% indium phosphide and 25% aluminum indium arsenide near the collector.

11. The HBT of claim 2, in which the tunneling suppression layer is formed of a digital alloy composite comprising aluminum gallium indium arsenide.

12. The HBT of claim 11, in which the digital alloy composite comprises $Al_{0.33}\,Ga_{0.15}\,In_{0.52}\,As$, using alternating layers of $Al_{0.48}In_{0.52}As$ and $Ga_{0.47}In_{0.53}$.

13. A method of making a heterojunction bipolar transistor, the method comprising:

providing a substrate;

forming a subcollector over the substrate;

forming a collector over the subcollector;

forming a tunneling suppression layer over the collector;

forming a base over the tunneling suppression layer; and

forming an emitter over the base,

wherein the tunneling suppression layer is formed using a material that is different from a material of the base and that has an electron affinity equal to or greater than an electron affinity of the material of the base.

14. The method of claim 13, further comprising forming the collector using indium phosphide, forming the base using gallium arsenide antimonide, forming the emitter using a material comprising two or more of indium, phosphorous, aluminum, gallium, nitrogen and arsenic, and forming the tunneling suppression layer using a material comprising two or more of aluminum, gallium, indium, nitrogen, phosphorous, arsenic and antimony.

15. The method of claim 14, further comprising forming the tunneling suppression layer using aluminum gallium indium arsenide.

16. The method of claim 15, in which the tunneling suppression layer comprises $Al_{0.33}Ga_{0.15}In_{0.52}As$.

17. The method of claim 15, in which the tunneling suppression layer consists essentially of $Al_{1-x-y}Ga_xIn_yAs$, where $0.09 \leq x \leq 0.25$, and $y=0.52$.

18. The method of claim 15, in which forming the tunneling suppression layer comprises forming the tunneling suppression layer with a graded electron affinity, χ.

19. The method of claim 18, further comprising forming the tunneling suppression layer essentially of $Al_{1-x-y}Ga_xIn_yAs$, where $0.09 \leq x \leq 0.25$, and $y=0.52$ and having greater a gallium mole-fraction near the collector than near the base.

20. The method of claim 14, further comprising forming the tunneling suppression layer using aluminum indium arsenide phosphide.

21. The method of claim 20, further comprising forming the tunneling suppression layer using indium phosphide and aluminum indium arsenide having 40% to 100% indium phosphide.

22. The method of claim 21, in which the tunneling suppression layer comprises indium phosphide and aluminum indium arsenide having 58% indium phosphide and 42% aluminum indium arsenide near the base and 75% indium phosphide and 25% aluminum indium arsenide near the collector.

23. The method of claim 14, further comprising forming the tunneling suppression layer using a digital alloy composite comprising aluminum gallium indium arsenide.

24. The method of claim 23, further comprising forming the digital alloy composite using alternating layers of $Al_{0.48}In_{0.52}As$ and $Ga_{0.47}In_{0.53}$.

25. A tunneling suppression layer, comprising two or more of aluminum, gallium, indium, nitrogen, phosphorous, arsenic and antimony.

26. The tunneling suppression layer of claim 25, comprising $Al_{0.33}Ga_{0.15}In_{0.52}As$.